VERSATILE METHOD AND SYSTEM FOR SINGLE MODE VCSELS

TECHNICAL FIELD OF THE INVENTION

The present invention relates, in general, to semiconductor lasers and, in particular, to a versatile system for producing single transverse mode Vertical-Cavity Surface-Emitting Lasers (VCSELs).

BACKGROUND OF THE INVENTION

The Vertical Cavity Surface Emitting Laser (VCSEL) is rapidly becoming a workhorse technology for semiconductor optoelectronics. VCSELs can typically be used as light emission sources anywhere other laser sources (e.g., edge emitting lasers) are used, and provide a number of advantages to system designers. Hence, VCSELs are emerging as the light source of choice for modern high-speed, short-wavelength communication systems and other high-volume applications such as optical encoders, reflective/transmissive sensors and optical read/write applications.

Surface-emitting lasers emit radiation perpendicular to the semiconductor substrate plane, from the top or bottom of the die. A VCSEL is a surface-emitting laser having mirrors disposed parallel to the wafer surfaces that form and enclose an optical cavity between them. VCSELs usually have a substrate upon which a first mirror stack and second mirror stack are disposed, with a quantum well active region therebetween. Gain per pass is much lower with a VCSEL than an edge-emitting laser, which necessitates better mirror reflectivity. For this reason, the mirror stacks in a VCSEL typically comprise a plurality of Distributed Bragg Reflector (DBR) mirrors, which may have a reflectivity of 99% or higher. An electrical contact is usually positioned on the second mirror stack, and another contact is provided at the opposite end in contact with the substrate. When an electrical current is induced to flow between the two contacts, lasing is induced from the active region and emits through either the top or bottom surface of the VCSEL.

VCSELs may be broadly categorized into multi-transverse mode and single-transverse mode, each category being advantageous in different circumstances. A goal in manufacturing single-mode VCSELs is to assume single-mode behavior over all operating conditions, without compromising other performance characteristics. Generally, the active regions of single transverse mode VCSELs require small lateral dimensions, which tend to increase the series resistance and beam divergence angle. Furthermore, a

device that is single-mode at one operating condition can become multi-mode at another operating condition, an effect that dramatically increases the spectral width and the beam divergence of the emitted radiation of the VCSEL.

Depending upon the application, the output mode of a VCSEL can either positively or negatively affect its use in signal transmission and other applications. The mode structure is important because different modes can couple differently to a transmission medium (e.g., optical fiber). Additionally, different modes may have different threshold currents, and can also exhibit different rise and fall times. Variation in threshold currents, which can be caused by different modes, combined with different coupling efficiencies of different modes can cause coupling into a transmission medium to vary in a highly non-linear manner with respect to current. Variable coupling to a transmission medium, combined with different rise and fall times of the various modes, can cause signal pulse shapes to vary depending on particular characteristics of the coupling. This can present problems in signal communications applications where transmission depends on a consistent and reliable signal. Other applications (e.g., printing devices, analytical equipment) may require a consistent and focused light source or spectral purity characteristics that render multiple mode sources inefficient or unusable.

Manufacturing a VCSEL with mode control and high performance characteristics poses a number of challenges. It is difficult to manufacture VCSELs that efficiently operate in the lower order mode (single mode). Most conventional VCSELs tend to lase in higher-order transverse modes, whereas single transverse mode lasing is preferred for some applications, such as sensors. Conventional attempts to produce a single mode VCSEL have generally resulted in structures having output power insufficient for practical use in most applications, as they remain single mode only over small current ranges. Usually, to manufacture a VCSEL, a relatively large current aperture size is required to achieve a low

series resistance and high power output. A problem with a large current aperture is that higher order lasing modes are introduced so that single mode lasing only occurs just above threshold, if at all. Manufacturing a VCSEL with a smaller current aperture to obtain single mode behavior causes multiple problems: the series resistance becomes large, the beam divergence angle becomes large, and the attainable power becomes small. Some conventional anti-guide structures may achieve this but suffer from manufacturing difficulties, particularly in requiring an interruption in epitaxial growth, a patterning step, and subsequent additional epitaxy. Other large single mode VCSELs require multi-step MBE or MBE/MOCVD combinations to manufacture, creating alignment and yield problems; increasing production costs and reducing commercial viability.

BRIEF SUMMARY OF THE INVENTION

The following summary of the invention is provided to facilitate an understanding of some of the innovative features unique to the present invention, and is not intended to be a full description. A full appreciation of the various aspects of the invention can be gained by taking the entire specification, claims, drawings, and abstract as a whole.

Therefore, a versatile system for producing a single mode VCSEL in a cost-effective and efficient manner, sustaining single mode operation over all current ranges is now needed, providing commercially viable VCSEL power output and performance while overcoming the aforementioned limitations of conventional methods.

In the present invention, electrical, thermal, and geometric optical properties of VCSEL components are designed and selected to provide current peaking in the center of a VCSEL device, coincident with the peak of the lowest order mode and to maximize loss in, or eliminate completely, higher order modes. Optionally, other mode control techniques can be used in conjunction with the teachings of the present invention to optically tailor the loss profile to prefer the fundamental mode.

The present invention provides structures and methods for producing a single mode VCSEL comprising a substrate, a bottom contact portion disposed upon a lower surface of the substrate, a lower mirror portion disposed upon an upper surface of the substrate, an active region disposed upon the lower mirror portion, and a current spreading upper mirror portion formed from electrically isotropic material and disposed upon the active region, an equipotential portion, which can include an additional mirror, disposed upon the upper current spreading mirror portion, an insulating layer interposed between the upper current spreading mirror portion and the equipotential portion and adapted to form an

aperture therebetween, and an upper contact portion disposed upon the equipotential layer outside the perimeter of the aperture.

The present invention provides a VCSEL component adapted to provided single mode operation over wide current ranges, comprising a semiconductor substrate having a lower surface and an upper surface, a bottom electrical contact disposed along the lower surface of the semiconductor substrate, a lower mirror formed of n-type material and disposed upon the upper surface of the semiconductor substrate, an active region having a plurality of quantum wells disposed upon the lower mirror portion, an upper current spreading mirror formed from electrically isotropic material and disposed upon the active region, an equipotential layer, which can include another mirror, disposed upon the upper mirror portion, a first upper electrical contact disposed upon the equipotential layer at a first lateral end of the VCSEL component, a second upper electrical contact disposed upon the equipotential layer at a second end of the VCSEL component at a particular distance from the first upper electrical contact, a first isolation region disposed beneath the first upper contact and traversing the equipotential layer, the upper mirror, the active region, and the lower mirror, a second isolation region disposed beneath the second upper contact and traversing the equipotential layer, the upper mirror, the active region, and the lower mirror, and an insulating layer interposed between the upper mirror and the equipotential layer and adapted to form therebetween an aperture.

The present invention further provides a method of providing antiguide mode selectivity in a VCSEL, including the forming of a VCSEL structure having a substrate, a bottom contact portion disposed upon a lower surface of the substrate, a lower mirror portion disposed upon an upper surface of the substrate, an active region disposed upon the lower mirror portion, and an upper current spreading mirror portion formed from electrically isotropic material and disposed upon the active region, providing a substantially

equipotential layer disposed upon the upper mirror portion, selectively interposing an electrically insulating layer between the upper mirror portion and the equipotential layer to form an aperture therebetween, wherein the electrically insulating layer is adapted to provide a greater nominal cavity resonance outside the aperture than inside it, and providing an upper contact portion disposed upon the equipotential layer.

The novel features of the present invention will become apparent to those of skill in the art upon examination of the following detailed description of the invention or can be learned by practice of the present invention. It should be understood, however, that the detailed description of the invention and the specific examples presented, while indicating certain embodiments of the present invention, are provided for illustration purposes only because various changes and modifications within the scope of the invention will become apparent to those of skill in the art from the detailed description of the invention and claims that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying figures, in which like reference numerals refer to identical or functionally-similar elements throughout the separate views and which are incorporated in and form part of the specification, further illustrate the present invention and, together with the detailed description of the invention, serve to explain the principles of the present invention.

FIG. 1 is an illustrative schematic of VCSEL component according to the present invention;

FIG. 2 is an illustrative diagram of the operation of the VCSEL component in FIG. 1;

FIG. 3 is an illustrative schematic of another VCSEL component according to the present invention;

FIG. 4 is an illustrative schematic of VCSEL component according to the present invention; and

FIG. 5 is an illustrative diagram of the operation of the VCSEL component in FIG. 4.

It should be understood that the drawings are not necessarily to scale and that the embodiments are illustrated using graphic symbols, phantom lines, diagrammatic representations and fragmentary views. In certain instances, details which are not necessary for an understanding of the present invention or which render other details difficult to perceive may have been omitted. It should be understood, of course, that the invention is not necessarily limited to the particular embodiments illustrated herein.

DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not delimit the scope of the invention.

It should be understood that the principles and applications disclosed herein can be applied in a wide range of optoelectronic applications. For purposes of explanation and illustration, the present invention is hereafter described in reference to VCSEL laser sources. However, the same system might be applied in other applications where a single mode source is utilized.

As previously discussed, one of the limitations of conventional single mode VCSEL approaches is their tendency to become multi-moded as current is increased, resulting in a very small effective current range and, hence, minimal power output, for single mode operation. Conventional VCSELs generally become multi-moded as current is increased because of current crowding near the edge of the emitting region and the resulting reduction in available gain in the center of the device, which is also caused by the sharp peaking of the lowest order mode in the center. This is true even for conventional devices having mode control structures.

In contrast, the present invention provides current peaked in the center of a VCSEL device, coincident with the peak of the fundamental (i.e., lowest order) mode. Optionally, other mode control techniques can be used in conjunction with the teachings of the present invention to optically tailor the loss profile to prefer the fundamental mode (e.g., use of long cavities, top surface patterning).

The present invention thus provides a single mode VCSEL having output power sufficient to meet the performance requirements of cost-sensitive commercial applications. Referring first to FIG. 1, a cross-sectional view of a VCSEL component 100 in accordance with the present invention is illustrated. VCSEL 100 comprises a substrate 102, formed of a suitable semiconductor material (e.g., Galium Arsenide [GaAs], Indium Phosphide [InP], or combinations thereof). VCSEL 100 further comprises a backside contact portion 104, formed of a suitable metallic or other conductive material, and adjoining a lower surface of substrate 102. A first semiconductor mirror stack 106 is disposed along the upper surface of substrate 102. Mirror 106 comprises a plurality of mirror pairs of alternating low and high refractive indexed material (e.g., DBR mirrors) and can be n-doped, for example. Disposed upon an upper surface of mirror 106 is active region 108. Active region 108 contains a number of quantum wells (e.g., three GaAs quantum wells). A second semiconductor current spreading mirror stack 110 is disposed along an upper portion of region 108 and can include a plurality of mirror pairs of p-doped material, for example. A conduction layer 112 is disposed atop and adjoining current spreading mirror 110. The resistivity of mirror 110 is much higher than in layer 112, and the conductivity of mirror 110 is as isotropic as possible. Layer 112 comprises a very high conductivity layer (e.g., 4 to 10 times the conductance of mirror 110) on top of mirror 110, which acts substantially like an equipotential (e.g., resistivity of about 0.01 ohm/cm). Layer 112 can comprise a highly doped semiconductor grown on the lower structures of VCSEL 100 (e.g., AlGaAs). Layer 112 can also comprise or include a DBR mirror structure. Alternatively, layer 112 can comprise a substantially equipotential portion of mirror 110. Because n-type mirrors typically have anisotropic conduction, it can be preferable to use a p-type material to form mirror 110. In VCSEL production processes where tunnel junctions produce nearly ohmic contact between n and p regions, without normal p-n junction characteristics, mirrors 106

and 110 can both be formed of either p-type or n-type material, as described hereafter in greater detail with reference to FIG. 4.

Generally, when the composition of any of the materials used comprises more than two chemical elements, that material's thermal conductivity decreases significantly. This increases thermal lensing while decreasing maximum power. It is thus desirable to use binary compositions, especially in proximity to region 108 (i.e., in mirrors 106 and 110).

VCSEL 100 further comprises a first electrical insulation region 114 and a second electrical insulation region 116, interposed between mirror 110 and conduction layer 112 in distally separate relation to one another, forming an aperture 118 between mirror 110 and layer 112. Although, as depicted in the cross sectional view of FIG. 1, regions 114 and 116 are separate structures, it is important to note that they can include segments of a single contiguous insulating region having the aperture (e.g., a circular aperture) formed therein. In this embodiment, there should be some electrical insulation between layer 112 and mirror 110, except for the area of aperture 118. This confines current flow toward the center of VCSEL 100. Optionally, regions 114 and 116 can be formed further within layer 110 (i.e., not immediately adjacent to layer 112), as described in later reference to FIG. 3. Insulation regions 114 and 116 can comprise an oxide, or some other suitable insulator available in the desired semiconductor process. The insulating regions can be any insulating material of any thickness (e.g., Al_2O_3 or air), but is optimal when reflectance of mirror 110, as measured from region 108, is minimized by the choice of thickness and position of the insulating regions. This causes more loss for higher order modes. Thus, the insulation regions can be designed or patterned to increase operational selectivity toward the fundamental mode. The thickness and positioning of the insulating regions can also be optimized such that the nominal cavity resonance outside the aperture 118 is at a longer wavelength than inside, providing an antiguide effect. Despite lower real indices

of materials such as Al_2O_3, proper thickness and positioning of the insulating regions will provide an effective higher index and result in a longer resonant wavelength. It is possible that, depending upon the processes and materials used, extended insulation areas may emanate from regions 114 and 116, having different electrical and optical effects on the performance of VCSEL 100. This phenomenon may be exploited to provide independent control of the optical and resistive effects, by altering the composition of the insulation regions (e.g., adding a proton implant to the regions).

VCSEL component 100 further comprises a first upper contact portion 120 and a second upper contact portion 122. Contacts 120 and 122 are formed of a suitable metallic or other conductive material atop conduction layer 112 in distally separate relation to one another, separated by a span 124. As depicted, regions 114 and 116 are formed beneath, and extending beyond, contacts 120 and 122, respectively, such that aperture 118 is smaller than span 124. Alternatively, contacts 120 and 122 and regions 114 and 116 can be formed such that contacts 120 and 122 overlap regions 114 and 116, resulting in an aperture 118 larger than span 124. As shown in FIG. 1, a first isolation region 126 is implanted beneath contact 120, traversing portions of layer 112, region 114, mirror 110, and region 108, and extending into mirror 106. Similarly, a second isolation region 128 is implanted beneath contact 122, traversing portions of layer 112, region 116, mirror 110, and region 108, and extending into mirror 106.

The conductivity and sheet conductance of layer 112 are many times (e.g., an order of magnitude) that of mirror 110. Layer 112 is formed of a thickness sufficient to enhance reflectivity of mirror 110. The lateral conductance of mirror 110 should be low, such that lateral current spreading is minimized. Mirror 110 and 112 are designed to have a phase relationship such that the combined structures provide maximum reflectivity inside aperture 118. Layer 112 provides mirror reflectivity because of its interface with the outside world.

Vertical conductance of mirror 110 should be high enough not to increase resistance excessively. Because the mirror stack is made of semiconductors of different band gaps, the mirror should be designed as isotropically conductive as is reasonable to reduce lateral current flow. As such, layers which have higher mobilities need lower doping, and layers with lower mobilities need higher doping, so that the resistivity is nearly the same all the way through and independent of direction. The product of the hole concentration and the mobility needs to be a constant for as much of mirror 110 as is possible. The interfaces between the semiconductors need to be doped more heavily and graded due to lower mobilities in the intermediate compositions of the grade and the modulation doping of lower gap material adjacent to wider gap material.

By forming an equipotential portion 112, and current spreading mirror 110 with the properties described above, and providing the current-restrictive aperture 118 therebetween, the present invention focuses the VCSEL current in the center of the device and at the lowest order mode, while minimizing and dispersing fringe current and effectively eliminating higher order modes. Mode selectivity is further provided by the antiguide effects of the present invention, as described above. FIG. 2 provides an illustration of advantages of the present invention. Indicators 200 depict operational current flow of VCSEL 100. The current density is maximized in the center portion 202 of VCSEL 100, coinciding with the peak of the lowest order mode. Current coinciding with higher order modes is widely dispersed, maximizing loss for those modes and effectively damping all but the lowest order mode. The present invention thus provides a single mode (i.e. the lowest order mode) VCSEL device, operational over a wide current range.

As previously indicated, a number of optional measures can be implemented to further increase modal selectivity in conjunction with the present inventions. Spacing and

thickness of the various component layers of VCSEL 100 can be varied to increase spreading effects (i.e., loss) of current associated with higher order modes (e.g., thickness of layers 114 and 116 can be increased). Additional structures can be added to VCSEL 100 to enhance optical selectivity. Referring back to FIG. 1, one such option is depicted in conjunction with VCSEL 100. A dielectric stack mode control structure is disposed atop layer 112. This structure comprises a first dielectric layer 130, disposed on an upper surface of layer 112 along span 124, and a second dielectric layer 132, disposed atop layer 130. Layer 132 can be positioned to align with aperture 118. Layer 130 is formed of a suitable material (e.g., SiO_2) with a thickness equivalent to one fourth (or some multiple thereof) the wavelength of light sourced by VCSEL 100. Layer 132 is formed of a suitable material (e.g., Si_3N_4) of a thickness, when combined with the thickness of layer 130, equivalent to one half (or some multiple thereof) the wavelength of light sourced by VCSEL 100. The effective mirror reflectivity under layer 130 is reduced and optical loss is increased, except for the area under layer 132, where the mirror reflectivity is either unaffected or enhanced, depending upon the material used to form layer 132. Thus, reflection back to the mirror under layer 132 is greater; and larger, higher order modes are suppressed. These effects can be combined with the other teachings of the present invention to further strengthen single mode selection and output.

Referring now to FIG. 3, a cross-sectional view of an alternative embodiment of a VCSEL component 300 in accordance with the present invention is illustrated. VCSEL 300 is substantially similar, in materials and construction, to VCSEL 100 of FIG. 1, with the exceptions detailed hereafter. VCSEL 300 comprises a substrate 302 and a backside contact portion 304 adjoining a lower surface of substrate 302. A first semiconductor mirror stack 306 is disposed along the upper surface of substrate 302. Disposed upon an upper surface of mirror 306 is active region 308. A second semiconductor mirror stack 310 is disposed along an upper portion of region 308, and a conduction layer 312 is disposed

atop and adjoining mirror 310. VCSEL 300 further comprises a first electrical insulation region 314 and a second electrical insulation region 316, medially interposed within mirror 310 between region 308 and conduction layer 312, in distally separate relation to one another, forming an aperture 318. VCSEL 300 can be so formed as long as peak gain and current density is realized toward the center of VCSEL 300. In this embodiment, the portion of mirror 310 above regions 314 and 316 (i.e., that portion directly adjacent to layer 312) should have as low a resistivity as is reasonable based on control constraints and free carrier absorption constraints.

As previously taught, heating must be prevented. Free carrier absorption causes a lot of heating in VCSEL devices. Heating can be minimized by having as low a doping at the electric field peaks as possible. I-R heating can become severe if doping is reduced excessively to reduce free carrier absorption. Keeping this in mind, reference is now made to FIG. 4, which presents an embodiment of the present invention addressing these concerns and building upon the teachings above.

FIG. 4 depicts a cross-sectional view of an embodiment of a VCSEL component 400 in accordance with the present invention. VCSEL 400 comprises a substrate 402, formed of a suitable semiconductor material (e.g., Galium Arsenide [GaAs], Indium Phosphide [InP], or combinations thereof). VCSEL 400 further comprises a first semiconductor mirror stack 404 disposed along the upper surface of substrate 402. Mirror 404 comprises a plurality of mirror pairs of alternating low and high refractive indexed material (e.g., DBR mirrors). AlGaAs DBR mirrors, using AlAs as the lower index extreme to improve thermal conductivity, can be utilized. Alternatively, AlInGaAsPSb, lattice matched to InP with a possible extreme composition of InP, can be utilized to improve thermal conductivity. Disposed upon an upper surface of mirror 404 is a first heat conduction layer 406. Layer 406 comprises a substrate-appropriate material (e.g., AlAs for GaAs substrates, InP for InP

substrates). Layer 406 is periodically doped to maximize doping at minima of electric fields and can be formed with a thickness on the order of one micron. This periodic doping can comprise doping heavily in the nulls of the electric field and doping lightly at the peaks of the electric field. The periodic doping improves conductivity and reduces the free carrier absorption. Use of uniformly heavy doping generally reduces series' resistance.

Disposed upon layer 406 is active region 408. Active region 408 comprises a lower p-n junction layer 410 disposed upon layer 406, a first tunnel junction 412 disposed upon layer 410, an upper p-n junction layer 414 disposed upon junction 412, and a second tunnel junction 416 disposed upon layer 414. Layers 410 and 414 can contain a number of quantum wells. By using tunnel junctions 412 and 416, a designer can then utilize n-type material in the mirror and heat conduction layers, providing significant reduction in free carrier absorption for a given conductivity. Within region 408, this is a particularly effective way to reduce currents and heating effects.

Disposed upon an upper surface of region 408 is a second heat conduction layer 418. Layer 418 is also isotropically formed as a current spreader. Layer 418 comprises a lightly doped substrate-appropriate material (e.g., AlAs for GaAs substrates, InP for InP substrates).

A second semiconductor mirror stack 420 is disposed above layer 418. Mirror 420 comprises a first upper mirror layer 422, a second upper mirror layer 424, and a third upper mirror layer 426. Layer 422 is formed to be as isotropic as possible and is lightly doped for free carrier absorption. Layer 422 can be formed to be of a thickness approximately equal to 4.5 periods. Layer 422 can comprise a plurality of mirror pairs of either n-doped or p-doped material, depending upon the process used, as previously noted. If n-type material is used, layer 422 can be formed above layer 424 (not shown). If layer 422 is

formed as shown in FIG. 4, layer 418 may be formed with a thickness of approximately one micron, for example. If layer 422 is formed above layer 424, then layer 418 should be thicker, formed with a thickness of approximately 2.6 microns, for example.

VCSEL 400 further comprises a first electrical insulation region 428 and a second electrical insulation region 430, interposed within layer 424 in distally separate relation to one another, forming an aperture 432 therebetween. The formation of aperture 432 confines current flow towards the center of VCSEL 400. As previously described, insulation regions 428 and 430 can comprise any appropriate insulating material of any thickness (e.g., an oxide) provided that they are formed toward minimizing reflectance of mirror 420, as measured from region 408, and also toward optimizing nominal cavity resonance to provide an antiguiding. Again, it is possible that, depending upon the processes and materials used, extended resistive regions 434 and 436 may emanate from regions 428 and 430, respectively, having different electrical and optical effects on the performance of VCSEL 400. As previously taught, regions 434 and 436 can be manipulated through design to provide independent optical and resistive control; however, generally, it is desirable that these regions are confined as narrowly as possible around the immediate area of regions 428 and 430.

Inside aperture 432, current density is higher than anywhere else, as is later illustrated in reference to FIG. 5. This current density causes significant IR heating, which must be prevented. Thus, layer 424 can comprise a heavily p-doped type material, or a moderately n-doped type material, or any other appropriate material (e.g., n-InP for an InP based VCSEL) that provides reduced series resistance and heating effects within aperture 432. Optionally, tapers 438 can be formed on the ends of regions 428 and 430, with tips positioned at electric field nulls, to enhance current confinement and mode selectivity. Layer 426 comprises a heavily doped material formed of appropriate thickness (e.g.,

approximately 16 periods for AlGaAs material) to optimize resistance and form, in relation to a conduction layer 440, an equipotential. Conduction layer 440 is disposed atop and adjoining mirror 420 and is formed of a very heavily doped material to minimize resistance. The resistivity of mirror 420 is higher than in layer 440, and the conductivity of mirror 420 is as isotropic as possible. Layer 440 comprises a very high conductivity layer on top of mirror 420, which acts substantially like an equipotential.

VCSEL component 400 further comprises a first upper contact portion 442 and a second upper contact portion 444. Contacts 442 and 444 are formed of a suitable metallic or other conductive material atop conduction layer 440 in distally separate relation to one another, separated by a span 124. VCSEL 400 can further comprise an appropriate mode selectivity structure 446, such as a dielectric mirror or mode control structure as previously described.

FIG. 5 provides an illustration of the current flow of VCSEL 400. Indicators 500 depict operational current flow of VCSEL 400. The current density is maximized in the center portion 502 of VCSEL 400, coinciding with the peak of the lowest order mode. Current coinciding with higher order modes is widely dispersed, maximizing loss for those modes and effectively damping all but the lowest order mode. As previously taught, the present invention thus provides a single mode (i.e. the lowest order mode) VCSEL device, operational over a wide current range.

The embodiments and examples set forth herein are presented to best explain the present invention and its practical application and to thereby enable those skilled in the art to make and utilize the invention. Those skilled in the art, however, will recognize that the foregoing description and examples have been presented for the purpose of illustration and example only. The teachings and concepts of the present invention can be applied to other

types of components, packages and structures, such as VCSEL components produced with other than a (100) orientation. The invention is applicable independent of a particular package configuration. Other variations and modifications of the present invention will be apparent to those of skill in the art, and it is the intent of the appended claims that such variations and modifications be covered. The description as set forth is not intended to be exhaustive or to limit the scope of the invention. Many modifications and variations are possible in light of the above teaching without departing from the spirit and scope of the following claims. It is contemplated that the use of the present invention can involve components having different characteristics. It is intended that the scope of the present invention be defined by the claims appended hereto, giving full cognizance to equivalents in all respects.